

UNITED STATES PATENT APPLICATION

for

INTEGRATED CIRCUIT PACKAGE

Inventors:

Brent Stone  
Kenneth Kassa  
Brian DeFord  
Erik Peter

Prepared by:

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP  
12400 Wilshire Boulevard  
Los Angeles, CA 90025-1026  
(303) 740-1980

File No.: 042390.P16890

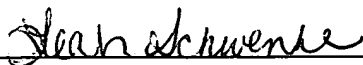
"Express Mail" mailing label number EV316318276US

Date of Deposit September 19, 2003

I hereby certify that this paper or fee is being deposited with the United States Postal Service "Express Mail Post Office to Addressee" service under 37 CFR 1.10 on the date indicated above and is addressed to the Commissioner of Patents and Trademarks, Washington, D.C. 20231.

Leah Schwenke

(Typed or printed name of person mailing paper or fee)

  
(Signature of person mailing paper or fee)

## **A MIXED PITCHED INTEGRATED CIRCUIT PACKAGE**

### **FIELD OF THE INVENTION**

[0001] The present invention relates to integrated circuits; more particularly, the present invention relates to integrated circuit packages.

### **BACKGROUND**

[0002] With the continued advancement of computer systems there is a desire to increase input/output (I/O) and power delivery interconnect performance, resulting in higher pin (or land) counts of socketed integrated circuit devices. Increasing the land (or pin) count of an integrated circuit typically results in increased package and socket size as the land pitch, the center to center spacing between lands, is uniform. An alternative method is to uniformly reduce the land pitch to minimize the impact of increasing the physical size of a device.

[0003] For a given socket technology, there is also a practical high volume manufacturing (HVM) limit restricting the extent to which socket land pitch can be reduced. At this time something larger than 1 mm in any dimension represents a HVM limit for various types of sockets (e.g., stamped metal contact land grid array (LGA) sockets). Therefore, if a target land count cannot be reached given a desired body size and the minimum HVM pitch limit, the only way to increase land count is to grow body size over the target. Growth to

package body size represents significant cost because all components of the total integrated circuit solution increase in cost.

[0004] Another limitation for increasing land count by reducing pitch is motherboard routing technologies used in breaking out signals from the socket. At this time, it is generally agreed that a 5mil line width and 5mil line-2-line space paired with a 25mil pad via and an 18mil socket pad represent the industry standard technology base for motherboard routing rules. The combination of these technologies with the desired signal to ground ratio for a device will limit how many rows deep land side motherboard breakout can reach. Non-land side breakout on the motherboard is limited by line geometries, via pad size, and via pitch.

## **BRIEF DESCRIPTION OF THE DRAWINGS**

[0005]        The present invention will be understood more fully from the detailed description given below and from the accompanying drawings of various embodiments of the invention. The drawings, however, should not be taken to limit the invention to the specific embodiments, but are for explanation and understanding only.

[0006]        **Figure 1** illustrates one embodiment of a motherboard, integrated circuit (IC) package and IC socket;

[0007]        **Figure 2** illustrates one embodiment of a motherboard, IC package with an unmated IC;

[0008]        **Figure 3** illustrates one embodiment of a motherboard, IC package with an IC package inserted into an IC socket;

[0009]        **Figure 4** illustrates one embodiment of a motherboard, IC package with a retention mechanism compressing the IC package into an IC socket;

[0010]        **Figure 5** illustrates a bottom view of one embodiment of an IC package with fixed (or uniform) pitch interconnect;

[0011]        **Figure 6** illustrates one embodiment of pitch definitions for motherboard technology baselines;

[0012]        **Figure 7** illustrates another embodiment of pitch definitions for motherboard technology baselines;

[0013]        **Figure 8** illustrates yet another embodiment of pitch definitions for motherboard technology baselines;

[0014]        **Figure 9** illustrates one embodiment of a motherboard breakout;

[0015]        **Figure 10** illustrates a partial top view of one embodiment of mixed row and columnar pitch stamped contact IC socket;

[0016]        **Figure 11** illustrates one embodiment of motherboard footprint with uniform, mixed pitch;

[0017]        **Figure 12** illustrates a top view of one embodiment of motherboard breakout for a uniform, mixed pitch IC socket;

[0018]        **Figure 13** illustrates a bottom view of one embodiment of motherboard breakout for a uniform, mixed pitch IC socket;

[0019]        **Figure 14(A)** illustrates a bottom view of one embodiment of a IC package with mixed pitch interconnect; and

[0020]        **Figure 14(B)** illustrates an isometric view of one embodiment of an IC socket with mixed pitch.

## DETAILED DESCRIPTION

[0021] An integrated circuit (IC) package with mixed pitch is described.

In the following description, numerous details are set forth. It will be apparent, however, to one skilled in the art, that the present invention may be practiced without these specific details. In other instances, well-known structures and devices are shown in block diagram form, rather than in detail, in order to avoid obscuring the present invention.

[0022] Reference in the specification to “one embodiment” or “an embodiment” means that a particular feature, structure, or characteristic described in connection with the embodiment is included in at least one embodiment of the invention. The appearances of the phrase “in one embodiment” in various places in the specification are not necessarily all referring to the same embodiment.

[0023] **Figure 1** illustrates one embodiment of a system 100. System 100 includes an IC package 130 mounted in a socket 120 on motherboard 110. Motherboard 110 is a physical arrangement in a computer system that includes the computer system's basic circuitry and components. On motherboard 110, circuitry is imprinted or affixed to the surface of a firm planar surface.

[0024] Socket 120 facilitates an electrical connection between IC 130 and circuits on motherboard 110. IC 130 is a semiconductor wafer on which thousands or millions of tiny resistors, capacitors, and transistors are fabricated. According to one embodiment, socket 120 is a zero insertion force (ZIF)

connector. However, in other embodiments, socket 120 may be implemented using other types of sockets (e.g., PGA). According to one embodiment, IC package 130 is a land grid array (LGA), with an accompanying LGA socket 120. However, in other embodiments, IC 130 may function as a pin grid array (PGA) or other type of microprocessor or IC circuitry with the accompanying PGA socket 120.

**[0025]**        **Figure 2** illustrates one embodiment of motherboard 110, LGA IC socket 120 with an unmated LGA IC 130. Motherboard 110 is coupled to solder balls 215. Solder balls 215 are coupled to land pads on motherboard 110 (not shown) to facilitate electrical contact at motherboard 110 for transmitting and receiving electrical signals.

**[0026]**        Contacts 225 are mounted on solder balls 215 as a component of socket 120 to provide a connection between motherboard 110 and IC package 130. In one embodiment, contacts 225 are stamped metal contacts. Lands 230 are mounted on package 130 to provide an electrical contact at package 130 for transmitting and receiving electrical signals.

**[0027]**        **Figure 3** illustrates one embodiment of IC package 130 manually inserted onto motherboard 110 via IC socket 120. In this embodiment, lands 230 physically connect with contacts 225, thus providing an electrical path between motherboard 110 and package 130.

**[0028]**        **Figure 4** illustrates one embodiment of IC package 130 manually inserted into IC socket 120 via a sustained compressive load. In such an

embodiment, a loading mechanism (not depicted) compresses package 130 into socket 120.

[0029] **Figure 5** illustrates a bottom view of one embodiment of an IC package 130. As shown in **Figure 5**, the lands on IC package 130 have a fixed distance (or pitch) between any two land centers in both the X and Y directions. As discussed above, there is a desire to increase I/O and power delivery interconnect performance through increased pin count.

[0030] However as described above, traditional socketed IC packages utilize a uniform (fixed) pitch that is maintained throughout the pinfield. Increasing pin counts with IC packages have been offset with scaling a fixed pitch to lower levels. Nonetheless, the cost of reducing pitch is becoming a significant challenge with fine pitched (<1.27mil) interconnects on large, low layer count printed circuit boards due to routing challenges.

[0031] Moreover, there are manufacturing and design constraints with a given socket technology that affect the pitch. Maintaining consistent row and/or column symmetry is desirable for manufacturing of stamped metal contact technologies. For stamped metal LGA contacts, a design constraint is introduced where the required contact deflection to mate with the IC package may limit the minimum pitch reduction in one direction "X" by a different amount than more than a perpendicular direction "Y"

[0032] **Figure 6** illustrates one embodiment of pitch definitions for motherboard technology baselines. Referring to **Figure 6**, IC land pads are



separated by a fixed distance, with a minimum distance between the land pads and the nearest trace. In addition, a minimum distance is maintained between each trace. Typically the distance between a land pad and a trace, and between traces, is 5 mil.

[0033]        **Figure 7** illustrates another embodiment of pitch definitions for motherboard technology baselines. In **Figure 7**, 25 mil land pads are shown, having a pitch of 50 mil. In between are 5 mil traces spaced at 5 mils apart.

**Figure 8** illustrates yet another embodiment of pitch definitions for motherboard technology baselines. In **Figure 8**, 18 mil land pads are shown, having a pitch of 43 mil, with 5 mil traces spaced at 5 mils apart.

[0034]        **Figures 7 and 8** show that the pitch between land pads may be reduced without sacrificing the minimum distance between land pads and traces. Thus, additional land pads may be placed on an IC. **Figure 9** illustrates one embodiment of a motherboard 110 breakout. Motherboard 110 includes land pads 915, with traces 950 coupled to pads 915 for signal routing. As described above, the breakout is limited by line geometries, via pad size, and pitch.

[0035]        According to one embodiment, motherboard 110, socket 120 and IC package 130 have a different pitches between various land pads, contacts and lands, respectively, to facilitate an optimal balance for increasing contact density with maintained socket manufacturability and accommodating lower cost motherboard 110 designs.

[0036]        **Figure 10** illustrates a partial top view of one embodiment of socket

120 having mixed row and columnar contacts 225. As shown in **Figure 10**, the vertical (X) and horizontal (Y) distances between contacts 225 are varied. **Figure 11** illustrates one embodiment of motherboard 110 footprint with uniform, mixed pitch. In one embodiment, the vertical pitch between land pads is 46 mil, while the horizontal distance is 43 mil.

[0037] **Figure 12** illustrates a top view of one embodiment of motherboard 110 breakout, on the land side of motherboard 110. **Figure 12** shows the routing of traces 950 to land pads 915 on motherboard 110. **Figure 13** illustrates a bottom view of one embodiment of motherboard 110 breakout on the non-land side of motherboard 110. **Figure 14(A)** illustrates a bottom view of one embodiment of a land grid array IC package with mixed pitch interconnect. **Figure 14(B)** illustrates an isometric view of one embodiment of a land grid array IC socket using stamped metal contacts with mixed pitch.

[0038] The mixed pitch between lands on an IC package increases contact density without requiring improved motherboard routing and socket manufacturing capabilities. The resulting increase in contact density allows for a smaller package, smaller socket, and a corresponding reduction in motherboard real estate, enabling for cost optimized components to be created without sacrificing performance.

[0039] Whereas many alterations and modifications of the present invention will no doubt become apparent to a person of ordinary skill in the art after having read the foregoing description, it is to be understood that any

particular embodiment shown and described by way of illustration is in no way intended to be considered limiting. Therefore, references to details of various embodiments are not intended to limit the scope of the claims which in themselves recite only those features regarded as the invention.